



Patent  
706316-1224

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Michael R. Butts

Serial No.: 10/669,095

Filed: September 23, 2003

For: Logic Multiprocessor For FPGA  
Implementation

)  
) **Group Art Unit:** Not Yet Assigned

)  
) **Examiner:** Not Yet Assigned

TRANSMITTAL OF FORMAL DRAWINGS

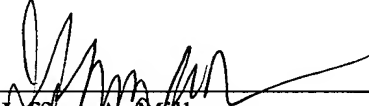
Commissioner for Patents  
Mail Stop: Patent Application  
P.O. Box 1450  
Alexandria, VA 22313-1450

Enclosed are the formal drawings (7 Sheets) for filing in the above-identified application.

Respectfully submitted,  
Orrick, Herrington & Sutcliffe LLP

Dated: February 27, 2004

By: \_\_\_\_\_

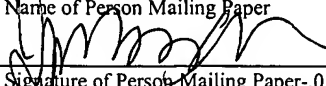
  
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(37 C.F.R. §1.8a)

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